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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/766,246	01/19/2001	Paul Garnett	5181-80100	8288

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EXAMINER
DANG, KHANH NMN

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/766,246	GARNETT, PAUL	
	Examiner	Art Unit	
	Khanh Dang	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/2/2002 Preliminary Amendment* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 10-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 10 and 11, the essential structural cooperative relationships between elements recited in the claim have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

In claim 12, lines 8-9, "[has an effect of masking]" should be deleted due to typing errors.

The subject matter of claims 17-20 cannot be ascertained because claims 17-20 are ambiguously constructed and not in conformation with US practice. The dependency of claim 17 is also unclear.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Klug et al.

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted and as best the examiner can ascertain, these claims do not positively define any structure/step that differs from Klug et al. With regard to claim 1, Klug et al. discloses a computer system comprising a plurality of processing sets (1-N), each having at least one processor, and a bridge (2, generally) coupled to each of processing sets (1-N) and operable to monitor a step locked operation of processing sets (1-N), wherein each of the processors has a processor identification register (10, 20, for example) which is read/writeable and is operable to store in said register data representative of a processor identification, said processors being arranged, consequent upon a predetermined condition, to load a common predefined data **value** that is common to said processing sets into said processor identification register (10, 20, for example). With regard to claims 2 and 3, see the condition of "reset" and "initialization" in Klug et al. With regard to claim 4, at least the instruction memory (7) is readable as the so-called "boot memory unit." With regard to claim 5, it is clear that instructions in ROM (7) is programmable. With regard to claim 6, it is clear that the contents of registers can also be both all zeros. With regard to claims 7-9, the information stored in each register (10, 20) can be used to identify processing set (1-N), and the predefined data is the matched data. With regard to claims 10 and 11, see explanation to claims 1 and 7-9 above. With regard to claims 12-15, one using the device of Klug et al. would have performed the same steps set forth in claims 12-15. See also "invalid match" in registers (10, 20) that causes error condition in Klug et al.

With regard to claims 16 and 17, it is clear that in Klug et al., any processing set (1-N) can be removed and replaced by another processing set, not necessarily identical to the removed one.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by GB 2290891 cited in the International Search Report.

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted and as best the examiner can ascertain, these claims do not positively define any structure/step that differs from GB 2290891 (891). With regard to claim 1, 7-11, 891 discloses a computer system comprising a plurality of processing sets (5 (a-d)), each having at least one processor, and a bridge (including identifier registers 26 to set a common value for each the processing sets) coupled to each of processing sets (1-N) and operable to monitor a step locked operation of processing sets (5 (a-d)), wherein each of the processors has a processor identification register (26, for example) which is read/writeable and is operable to store in said register data representative of a processor identification, said processors being arranged, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said processor identification register (26, for example). With regard to claims 2 and 3, see the condition of "reset" and "initialization" in 891. With regard to claims 4 and 5, the "initiallisation program" stored in ROM 13 is readable as the so-called "boot memory unit." With regard to claim 6, it is clear that the

in 891, all register contents can be initialized to zeros by reset signal line 35, for example. With regard to claims 12-15, one using the device of 891 would have performed the same steps set forth in claims 12-15. See also "fault" condition described in detail in 891, that causes error condition. With regard to claims 16 and 17, it is clear that in 891, any processing set (5(a-d)) can be removed and replaced by another processing set, not necessarily identical to the removed one.

U.S Patent Nos. 5,991,900 to Garnett, 5,175,847 TO Mellot, and 6,473,869 to Bissett et al. are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner